

IN THE CLAIMS

Please amend the claims as follows.

1-8 (Cancelled)

- 1 9. (Previously presented) An integrated circuit comprising:
 - 2 a register file bit comprising:
 - 3 a primary latch having a data input and a data output;
 - 4 a plurality of secondary latches each having a data input and a data output;
 - 5 a feedback path from the data outputs of the plurality of secondary latches
 - 6 to the data input of the primary latch, the feedback path including a data selection
 - 7 mechanism for selecting one data output only from among each of the data
 - 8 outputs from the plurality of secondary latches to feed back to the data input of the
 - 9 primary latch; and
 - 10 a context switch mechanism that causes the data on the data output of the
 - 11 primary latch to be written to a selected one of the plurality of secondary latches,
 - 12 and that causes the data on the data output of the selected one secondary latch to
 - 13 be written to the primary latch.
- 1 10. (Currently amended) The integrated circuit of claim 9 wherein the context switch
- 2 mechanism comprises a swap signal coupled to gate control input on the primary latch.
- 1 11. (Original) The integrated circuit of claim 9 wherein the context switch mechanism
- 2 comprises a delay element between the data output of the primary latch and the data
- 3 inputs of the plurality of secondary latches.
- 1 12. (Original) The integrated circuit of claim 9 wherein the context switch mechanism
- 2 comprises a delay element in the feedback path.

- 1 13. (Original) The integrated circuit of claim 9 wherein the context switch mechanism
 - 2 comprises at least one clock signal that latches data on the data input of the primary latch
 - 3 to the data output of the primary latch and at least one clock signal that latches data on the
 - 4 data input of a secondary latch to the data output of the secondary latch.
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- 1 14. (Original) The integrated circuit of claim 9 further comprising a plurality of write
 - 2 ports on the data input of the primary latch.
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- 1 15. (Original) The integrated circuit of claim 9 further comprising a plurality of read ports
 - 2 on the data output of the primary latch.

16-20 (Cancelled)

1 21. (Currently amended) A method for performing a fast context switch in a register file
2 that includes a primary latch and a plurality of secondary latches having data outputs, the
3 method comprising the steps of:

4 (A) for each a selected one secondary latch of the plurality of secondary latches,
5 performing the steps of A1 and A2:

6 (A1) storing a first value in the primary latch that corresponds to a selected
7 thread;

8 (A2) moving the first value in the primary latch to [[a]] the selected one of
9 the plurality of secondary latches;

10 (B) storing a second value in the primary latch that corresponds to an active
11 thread;

12 (C) selecting [[one] a data output of the selected one secondary latch only from
13 among each of the data outputs of the secondary latches for performing a context switch
14 with the primary latch; and

15 (D) performing a context switch between the primary latch and the selected one
16 secondary latch that causes the second value in the primary latch to be stored in the
17 selected one secondary latch, and that causes the first value in the selected one secondary
18 latch to be stored in the primary latch.

1 22. (Cancelled)

STATUS OF THE CLAIMS

Claims 1-22 were originally filed in this patent application. In the previous office action, claim 9 was objected to for an informality and claims 1-17 and 19-22 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,831,623 to Terzian. No claim was allowed. In the first response dated 04/20/2006, claims 1, 8, 16, 19 and 21 were amended and claim 18 was cancelled. A second response dated 08/02/2006 was not entered by the examiner. In an amendment filed with a request for continued examination on 09/25/06, claims 9 and 21 were amended and claims 1-8, 16-17 and 19-20 were cancelled. In the pending office action, claims 9-15, 21 and 22 were rejected under 35 U.S.C. §112 second paragraph. Further, claims 9-15 and 21-22 were rejected under 35 U.S.C. §102(b) as being anticipated by Henry. In the current amendment, claims 10 and 21 were amended and claim 22 was cancelled. Claims 9-15 and 21 are currently pending.